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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,081	06/25/2003	John W. Horigan	42P16970	6540

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EXAMINER

HOLTON, STEVEN E

ART UNIT PAPER NUMBER

2629

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,081	HORIGAN, JOHN W.	
	Examiner	Art Unit	
	Steven E. Holton	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 January 2006.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-8,10-14 and 16-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-8,10-14 and 16-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is made in response to applicant's amendment filed on 1/18/2006. Claims 1,2, 4-8, 10-14, and 16-20 are currently pending in the application. An action follows below:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 2, 8, and 14 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for two different embodiments one involving using a predetermined threshold for generating a feedback signal to correct the clock signal and a second method involving using a counter to count clock pulses and using the difference between clock pulses to correct the clock signal (page 8, lines 4-16), does not reasonably provide enablement for a combined method of feedback using both of these methods. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. In light of the specification one skilled in the art would not understand why or how to utilize both feedback methods described in a single combined embodiment. As is shown in the specification, the two methods are intended to provide different embodiments and the combination of the two would cause miscommunication or unneeded redundancy within the system. If the different between

Art Unit: 2629

clock pulses occurs before reaching the predetermined threshold then the threshold correction method would never be reached, or the opposite, if the predetermined threshold was reached before the difference in clock pulses was great enough, the clock signal counter would be never be required. It might also be possible that both systems send feedback signals at almost simultaneous times, which may cause a cancellation of the feedback signal or overcompensation and drive the problem towards the other extreme. The amendments to the claims have caused this combination error by overlapping two previously distinct and separate embodiments into a single invention that is unsupported by the specification.

Claim Rejections - 35 USC § 103

✓ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 4-7, 10-13, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants Admitted Prior Art (paragraphs 4-6 of the disclosure), hereinafter AAPA, in view of Chao et al. (USPN: 5007070), hereinafter Chao.

Regarding claim 1, AAPA discloses a prior method of generating a pixel stream from a non-SSC clock (paragraph 5, lines 1-2) and forwarding a second clock signal and the first pixel stream to a buffer to translate the first pixel stream based on the

Art Unit: 2629

second clock signal (paragraph 5, lines 2-4). The Examiner notes that the AAPA does not expressly state if the clocks come from one or two sources, the use of two sources would be obvious to one skilled in the art. However, AAPA does not expressly disclose providing a feedback to the second source to cause the second source to adjust the center frequency of the second clock signal to match the average frequency of the first clock signal with the average frequency of the second clock signal.

Chao discloses a feedback system to correct differences in frequency between two clock sources (col. 3, lines 3-11). The two clock sources being an input clock coupled to an incoming data stream and the output clock source (Fig. 7A, element 180) for reading data out of a buffer. The frequency of the output clock source is changed depending on the difference between the measured clock pulses (Fig. 7b; col. 11, line 30 – col. 12, line 4).

At the time of invention, it would have been obvious to one skilled in the art to combine the teachings of AAPA and Chao to produce a clock system with feedback based on the difference of counts of two clock pulses to correct the frequency of the second clock signal. The motivation for doing so would have been “to provide a clock recovery circuit which can recover a clock from information which does not arrive at predetermined times and which is bursty (Chao, col. 2, lines 51-55).” Thus, it would have been obvious to one skilled in the art that the method of counting clock pulses and using the difference between clock pulses to alter clock frequencies to match described by Chao could be used in a graphics system as described by AAPA. The combination of the two would produce a method as described in claim 1.

Regarding claim 4, Chao discloses using a voltage controlled oscillator (Fig. 7A, element 180, described in col. 11, lines 4-18 as element 18). The examiner notes that the voltage controlled oscillator output connected as feedback to the comparison circuit to alter the frequency of the oscillator is a phase locked loop.

Regarding claim 5, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 6, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8) and a pixel stream associated with the spread spectrum clock signal to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 7, the Examiner notes that this is an apparatus to be operated using the associated method of claim 1. Although there is no provided figure of a display system that would operate as described by AAPA, the Examiner states that the system would inherently possess a first and second circuitry to produce first and second clock signals; a display pipe to generate a first pixel stream based on the first clock signal; and a buffer coupled to the display pipe to receive the first pixel stream and the second clock signal to transform the first pixel stream into a second pixel stream on the second clock signal. The Examiner notes that no specific mention of a display pipe is made in the AAPA, but there would inherently be some device to produce the pixel stream and such a device could be a display pipe, which is known in the art. AAPA does not expressly disclose the second circuitry being coupled to the buffer to receive a

Art Unit: 2629

feedback, to adjust the center frequency of the second clock signal and a counter circuit used to produce the feedback signal.

Chao discloses, “a second circuitry coupled to the buffer to generate the second clock signal and to receive feedback to adjust the center frequency of the second clock signal (Fig. 5, element 80 is coupled to element 68, the buffer)”. The voltage controlled oscillator (Fig. 7A, element 180 (described as element 18 in the disclosure)) produces the clock signal, rd and receives feedback from the phase detector (Fig. 7a, element 150). The phase detector described by Chao can be equated to the counter described in the claims. The phase detector is coupled to the first clock circuitry (Fig. 5, element 78) and the second clock circuitry (Fig. 7a, element 180) and counts the clock pulses of each signal (Fig. 7B, elements 171 and 172) and produces feedback when the number of clock edges between the two signals differs for a period of time (col. 11, line 19 – col. 12, line 4).

At the time of invention, it would have been obvious to one skilled in the art to combine the teachings of AAPA and Chao to produce a clock system with feedback based on the difference of counts of two clock pulses to correct the frequency of the second clock signal. The motivation for doing so would have been “to provide a clock recovery circuit which can recover a clock from information which does not arrive at predetermined times and which is bursty (Chao, col. 2, lines 51-55).” Thus, it would have been obvious to one skilled in the art that the method of counting clock pulses and using the difference between clock pulses to alter clock frequencies to match described

Art Unit: 2629

by Chao could be used in a graphics system as described by AAPA. The combination of the two would produce a device as specified in claim 7.

Regarding claim 10, Chao discloses using a voltage controlled oscillator (Fig. 7A, element 180, described in col. 11, lines 4-18 as element 18). The examiner notes that the voltage controlled oscillator output connected as feedback to the comparison circuit to alter the frequency of the oscillator is a phase locked loop.

Regarding claim 11, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 12, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8) and a pixel stream associated with the spread spectrum clock signal to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 13, the Examiner notes that the claim is drawn to a system comprising the device of claim 7 coupled to dynamic random access memory. Therefore, the arguments of claim 7 can be applied to the similar components of claim 13. Regarding the dynamic random access memory, the Examiner states that in a computer system which is what the graphics apparatus of claim 7 would be used in dynamic random access memory (DRAM) would be an inherent and obvious part of the computer system. DRAM is conventionally used to store program and graphics information in an operating computer system and having it coupled to the graphics controller of claim 7 would be an obvious choice for one skilled in the art.

Thus, the addition of DRAM to the device of claim 7 would have been obvious to one skilled in the art to provide storage for graphics information that would be used by the apparatus of claim 7 to produce pixel streams and other operating information for the computer system.

Regarding claim 16, Chao discloses using a voltage controlled oscillator (Fig. 7A, element 180, described in col. 11, lines 4-18 as element 18). The examiner notes that the voltage controlled oscillator output connected as feedback to the comparison circuit to alter the frequency of the oscillator is a phase locked loop.

Regarding claim 17, AAPA discloses using a non-spread spectrum modulation clock signal (paragraph 5, lines 1-2) and a spread spectrum modulation clock signal (paragraph 5, lines 2-3).

Regarding claim 18, AAPA discloses sending the pixel stream associated with the spread spectrum clock signal [second pixel stream] to a liquid crystal display panel (paragraph 4, lines 3-4).

Regarding claim 19, AAPA discloses sending the pixel stream associated with the non-spread spectrum [first pixel stream] to a cathode ray tube display (paragraph 4, lines 6-8).

Regarding claim 20, the Examiner notes that the graphics memory controller hub is used within a computer system. As such, it would be obvious to one skilled in the art that the hub would be coupled to a processor that is part of the external computer system. The external processor would be in charge of the computer functions and programs running on the computer.

Response to Arguments

4. Applicant's arguments, see pages 8-11, filed 1/18/2006, with respect to the rejection(s) of claim(s) 1-20 under 35 USC 103 have been fully considered and are persuasive in light of the arguments and amendments to the claims. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

Regarding the Applicants arguments over presentation of information regarding the use of dynamic random access memory ("DRAM") in the computer systems, the Examiner provides Foster et al. (USPN: 5551033) who discloses a laptop computer system with a processor and main memory, the main memory described as being DRAM (col. 6, lines 11-14). The Examiner also notes that DRAM was invented in 1970 and first used in computer systems in the HP 9800 series of computers ("Inventors of the Modern Computer"; <http://inventors.about.com/library/weekly/aa100898.htm>), which were first produced in 1972 ("HP 9800 Series Computers Description"; <http://www.classiccmp.org/hp/9800.htm>). Thus, computer systems with dynamic random access memory are commonly known in the art.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Foster et al. (USPN: 5551033) discloses a computer system using dynamic random access memory.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571) 272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2629

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven E. Holton
April 7, 2006
Division 2629

AMR A. AWAD
PRIMARY EXAMINER

